Online Winter Faculty Development Programme Intricacies of Analog & Mixed Signal design

February 17 - 28, 2025 (04:00 PM-08:00 PM) live streaming

Jointly Organized by

NIT Warangal





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and hosted by **IIIT Nagpur**



In association with **Electronics and ICT Academy**

Pandit Dwarka Prasad Indian Institute of Information Technology, Design and Manufacturing, Jabalpur

Schedule and Course Contents

- Basic MOS Device Physics, Amplifiers- differential amplifiers, frequency response of amplifiers- common source/gate, Cascode, CMRR, Gilbert cell, Miller effect, Noise in amplifiers, current mirrors, OpAmp- multistage, OTA, stability & frequency compensation.
- Sample and Hold Circuits: Basic S/H circuit, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H, D/A Converter: - General considerations, Static non-idealities and Dynamic non-idealities; Current-steering DAC -Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches.
- A/D converter: General considerations, static and dynamic non-idealities. Flash ADC Basic architecture, Design issues, Comparator and Latch, Effect of non-idealities, Interpolative and Folding architectures. Successive Approximation ADC; Pipeline ADC. Over sampling ADC - Noise shaping, Sigma-Delta modulator, PLLs: Basic Phase-Locked Loop Architecture.
- ■Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Liberalized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-Order Small Signal Model, PLL Design Example.

Coordinators

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RESOURCE PERSONS

- Prof. Sreehari rao patri, NITW
- Prof Gjendranadh, IITH
- Prof Saurabh Saxena, IIT Madras
- Prof Kapil Jainwal, IITH
- Dr Chitra, IIT Kanpur
- Prof Nagendra, IITM

Registration Details

Registration link - Please fill in the registration form using the following link:

https://forms.gle/GcEGxbJ9d1xSQTj98

Registration fee: INR 500/-

Last Date for Registration: February 15 2025

Contact Details

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Online payment details:

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